

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

**METHOD FOR FABRICATING MERGED LOGIC CMOS DEVICE**

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## METHOD FOR FABRICATING MERGED LOGIC CMOS DEVICE

### Technical Field

5 A merged logic CMOS device is disclosed, and more particularly, a method for fabricating a merged logic CMOS device is disclosed which simplifies the process by forming a deep junction in a double diffused drain (DDD) structure using a retrogradated well ion implantation process.

### Description of the Related Art

10 Generally, in a high voltage external system that is controlled by an integrated circuit, the integrated circuit must require a device for controlling the high voltage. In addition, circuits in need of a high breakdown voltage also require a specific device for controlling the high voltage.

15 Examples of devices requiring such high voltage control include liquid crystal displays (LCD), devices for driving fluorescence indicator panels (FIP) or the like.

20 For an external system to which a high voltage is directly applied, in order to smoothly drive the external system with a driving transistor, the voltage should be greater than the breakdown voltage of the high voltage applied between the drain with the high voltage applied to the semiconductor substrate. Further, in order to increase the breakdown voltage, the concentration of impurities in the substrate should be lowered.

25 Thus, to obtain a high breakdown voltage, a double diffused drain (DDD) structure having the same conductive type lightly-doped region as a source and a drain is formed at a lower part of the source and drain regions. With such a structure, it is possible to obtain a high breakdown voltage as well as prevent a hot carrier effect.

30 Such a hot carrier effect is described as follows. A strong electric field is formed at a channel region around a drain as the length of the channel becomes smaller. As a result, a hot carrier with an accelerated high energy is trapped toward the gate generating a loss caused by leakage, and the gate oxide is damaged thereby decreasing the threshold voltage.

In a conventional high voltage device, a junction breakdown voltage of the high voltage device is determined according to the junction length or concentration of a source or drain, so the source/drain must be formed in a double diffused drain (DDD) structure. For this purpose, it is necessary to form a 5 source/drain with a deep junction and a low concentration. This can be implemented by diffusion at a high temperature for an extended period of time.

However, the process of forming a conventional high voltage device has the following problems.

In the conventional art implementing a DDD structure of a high 10 voltage device, since the diffusion is repeated, a low voltage driving has to be conducted. When implementing the DDD structure along with a CMOS logic device with a shallow junction structure, degradation of the characteristics of the logic device will result.

In order to design a process in such a way as to affect the logic device 15 as little as possible, the number of process steps is greatly increased.

This leads to a problem in that productivity is lowered and manufacturing costs are increased.

#### **SUMMARY OF THE DISCLOSURE**

In consideration of the problems of the fabrication process of a merged 20 logic device of the prior art, a method for fabricating a merged logic device is disclosed which simplifies the process by forming a deep junction of a double diffused drain (DDD) structure by a retrograded well ion implantation process upon forming a high voltage device.

A disclosed method for fabricating a merged logic device comprises: forming a high voltage p-type well region on a semiconductor substrate; conducting an ion implantation for forming a logic p-type well region on a logic region and a field stop ion implantation; forming a logic well region in the high voltage p-type well region; forming a high voltage gate oxide film on the entire surface and conducting a 30 threshold voltage ion implantation process; forming a logic gate oxide film in the logic region and simultaneously forming a logic gate electrode and a high voltage gate electrode; forming a logic LDD region in the logic region and forming a spacer on the sides of the gate electrodes; and forming logic source/drain regions, high voltage source/drain regions and a bulk bias control region.

## BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects of the disclosed methods will become apparent from the following description with reference to the accompanying drawings, wherein

5 Figs. 1a to 1f are cross sectional views showing the process of  
fabricating a merged logic device according to this disclosure.

## DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

Hereinafter, preferred embodiments will be described in greater detail  
10 while referring to the drawings.

Figs. 1a to 1f are cross sectional views showing the process of  
fabricating a merged logic device according to this disclosure.

The disclosed methods permit a decrease in the number of process  
steps over conventional high voltage fabrication processes by simplification of the  
15 fabrication process. The disclosed methods also lower the degree of degradation of  
the characteristics of the logic device.

In a DDD structure of a source/drain of a prior art high voltage device,  
a heating cycle for implementing a deep junction is substituted for the retrograded  
well ion implantation process.

20 In contrast, by using the disclosed retrograded well ion implantation  
process, the number of process steps is decreased, and this process is superior from  
the viewpoint of throughput and efficiency.

Firstly, as shown in Fig. 1a, a device isolation layer 13 is formed on a  
semiconductor substrate 11 to define a logic region 30. Also, a high voltage p-type  
25 well region 12 is formed in the semiconductor substrate 11 to define a high voltage  
device-forming region 31.

Simultaneously, as shown in Fig. 1b, a high voltage n-type well region  
15 for forming source/drain regions of the high voltage device is formed on the high  
voltage p-type well region 12 while a logic p-type well region 14 formed on the logic  
30 region 30.

In this way, the logic well region 32 and the high voltage device forming region 31 is continuously formed with the formation of the logic p-type well region 14 and the high voltage n-type well region 15. A field stop layer 33 may also be formed at this time. Thus, a basic structure of the high voltage device formed 5 without a high temperature diffusion process.

Further, as shown in Fig. 1c, a high voltage gate oxide film 16a is formed on the entire surface, and a threshold voltage ion implantation of the logic region 32 and a threshold voltage ion implantation of the high voltage device region 31 are conducted.

10 Next, as shown in Fig. 1d, by a wet etching process, the high voltage gate oxide film 16a of a logic region is removed and a logic gate oxide film 16b is formed.

15 And, a gate forming material layer is formed on the entire surface and selectively etched to form a logic gate electrode 17a and a high voltage gate electrode 17b.

Next, as shown in Fig. 1e, lightly-doped n-type impurity ions are implanted into the logic region to form a logic DDD region 18.

20 And, as shown in Fig. 1f, a spacer 22a is formed on the sides of the logic gate electrode 17a and a spacer 22b is formed of the high voltage gate electrode 17b, and logic source/drain regions 19, high voltage source/drain regions 20 and a 25 bulk bias control region 21 are formed by an ion implantation process.

Hereto, although a method for fabricating a high voltage (HV) PMOS has been described, it is also possible to fabricate a NMOS transistor by the same method as this PMOS fabrication method.

According to the disclosed process, in the fabricating of a high voltage device employed for the applications of TFT LCD driver ICs, mobile phones, display (color STN, OLED) products and the like of which demand for is rapidly increasing, it is possible to reduce the fabrication cost and prevent the degradation of the characteristics of the logic device by employing the implementation method of a basic 30 CMOS logic device.

The forgoing process is merely exemplary and is not to be construed as limiting this disclosure. The teachings can be readily applied to other types of apparatuses. The description of the disclosed process is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and 5 variations will be apparent to those skilled in the art.

The method for fabricating a merged logic device according to the disclosed as described above has the following effects.

First, the stable characteristics of the logic device can be acquired by greatly reducing the number of steps of thermal diffusion required for implementing a 10 high voltage transistor.

Second, since the number of process steps required for implementing the high voltage transistor is reduced, the process can be simplified, the fabrication costs lowered, and the throughput improved.

Third, it is possible to improve the shortage of a short channel margin 15 caused by thermal diffusion on the sides of the high voltage source/drain by reducing diffusion.